INTEGRATED CIRCUITS

DATA SHEET

TDA8730
PLL FM demodulator for DBS signals

Preliminary specification
File under Integrated Circuits, IC02

March 1991

Philips Semiconductors

PHILIPS

PLL FM demodulator for DBS signals TDA8730

FEATURES

- Broadband IF amplifier
- PLL demodulator, consisting of:
  - a multiplier
  - a voltage controlled oscillator
  - a loop amplifier
- AGC detector and DC amplifier
- LOW impedance video and data output
- Power supply voltage stabilizer

GENERAL DESCRIPTION

The TDA8730 is a sensitive PLL demodulator for the second IF and direct broadcasting satellite (DBS) receivers. It provides AGC output and threshold adjustment for optimal signal level at the input of the demodulator.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		–	9	–	V
I_{DD}	supply current		–	75	–	mA
V_I	input voltage level		–	70	–	dBμV
f_{osc}	minimum oscillator frequency		–	130	–	MHz
f_{osc}	maximum oscillator frequency		–	720	–	MHz
V_O	video output signal amplitude (peak-to-peak value)	note 1	–	1.1	–	V
V_{AGC}	AGC output voltage		1.8	–	V_{DD}	V

Note

1. Δf = 13.5 MHz (peak-to-peak value)

ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8730	16	DIL	plastic	SOT38GE(1)

Note

1. SOT38-1; 1996 December 4.

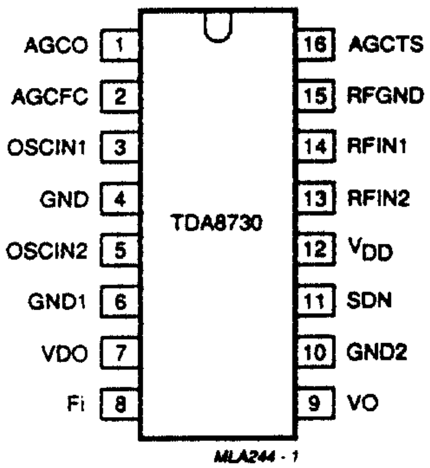


Fig.1 Pinning diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
AGCO	1	AGC output
AGCFC	2	AGC frequency compensation
OSCIN1	3	oscillator input 1
GND	4	GND
OSCIN2	5	oscillator input 2
GND1	6	ground 1
VDO	7	variable capacitor drive output
FI	8	feedback input
VO	9	video output
GND2	10	ground 2
SDN	11	stabilizer decoupling node
V_{DD}	12	supply voltage +9 V
RFIN2	13	RF input 2
RFIN1	14	RF input 1
RFGND	15	RF ground
AGCTS	16	AGC threshold setting

APPLICATIONS

Direct broadcasting satellite (DBS) receivers.

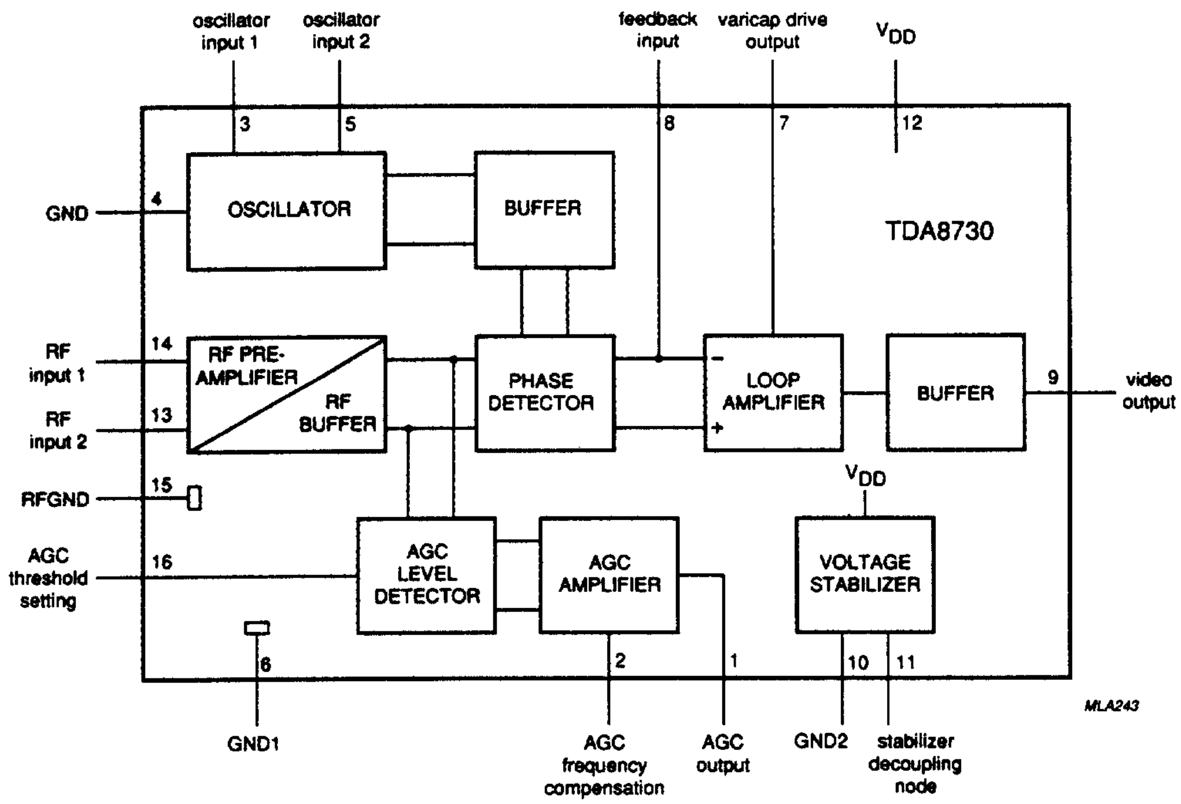


Fig.2 Block diagram.

FUNCTIONAL DESCRIPTION

The TDA8730 is a PLL FM demodulator intended for use in satellite tuners. It can demodulate frequency deviations ranging from 13.5 $MHz_{(p-p)}$ (DBS services) up to 25 MHz(p-p) (FSS services) and offers a high demodulation linearity. The circuit is optimized for operation at 479.5 MHz (the European IF for satellite tuners) and can handle the various broadcasting standards that are in use (including MAC).

Due to the PLL principle, demodulation noise threshold extension is possible. The high sensitivity of the balanced IF input reduces the additional gain, required in the tuner.

An on chip AGC circuit delivers a gain control signal for use by the tuner IF amplifier, and a voltage regulator makes the circuit insensitive supply voltage changes.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	–0.3	11	V
I_{DD}	input voltage	–0.3	V_{DD}	V
$I_{O(source)}$	output source current	–	10	mA
V_{AGC}	AGC output voltage	–	11	V
t_{sc}	max short circuit time of outputs	10	–	s
$V_{AGC(adj)}$	AGC threshold adjustment voltage	–0.3	V_{DD}	V
T_{stg}	storage temperature	–55	150	°C
T_j	junction temperature	–	150	°C
T_{amb}	operating ambient temperature	–25	85	°C

THERMAL RESISTANCE

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
$R_{th\ j\text{-}a}$	from-junction-to-ambient in free air	55	–	K/W

CHARACTERISTICS

V_{DD} = 9 V; T_{amb} = 25 °C; f = 480 MHz; Input level 70 dBμV; measured in circuit of Fig.4 unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage	$V_{pin\ 12}$ to pin 10 or pin15	8.1	9.0	9.9	V
I_{DD}	supply current	$I_{pin\ 12}$; note 1	–	75	90	mA
Frequency demodulator						
f_{osc}	minimum oscillator frequency	–	–	130	–	MHz
f_{osc}	maximum oscillator frequency	–	–	720	–	MHz
V_i	operating input level	pin 13; note 2	–	70	74	dBμV
S11	input reflection coefficient |S11| unbalanced; pin 14 decoupled (50 Ω reference)	pin 13; note 3	–	0.07	–	
	balanced; 100 Ω reference	pin 13 to pin 14	–	0.11	–	
Kd	phase detector constant	(level at pin 13 is 70 dBμV)	–	0.45	–	V/rad.
Ko	VCO constant		–	12	–	MHz/V
Ao	open loop gain of loop amplifier	pin 7 to pin 8	–	40	–	dB
f-3 dB	open loop bandwidth of loop amplifier		–	2.8	–	MHz
Z_{in}	input impedance of feedback input	pin 8	–	930	–	Ω
Z_{out}	output impedance of loop amplifier	pin 7	–	30	50	Ω
le	VCO linearity error over Δf = ±10 MHz	note 4	–	1	–	%
	shift of DC level at video output for ΔV_{DD} = ±10% with unmodulated 480 MHz input signal	pin 9	–	–	±50	mV
	drift of DC level at video output for T_{amb} = 25 to 50 °C with unmodulated 480 MHz input signal	pin 9	–	–	+50	mV
V_{VCO}	VCO capture range		±14	–	–	MHz
G_d	differential gain	note 5	–	–	±4	%
ϕ_d	differential phase	note 5	–	–	±2	deg.
MOD	intermodulation	note 6	–	–70	–	dB
AGC						
V_{IAGC}	AGC threshold (IAGC = 0 mA) as a function of voltage applied to pin 16 V_{pin16} = 0.8 V	pin 13	–	–	67	dBμV
	$V_{pin\ 16}$ = 9.0 V	note 7	73	–	–	dBμV
	AGC steepness	pin 1; note 8	–	18	–	mA/dB
	AGC output saturation voltage HIGH at I = –0.2 mA	$V_{pin\ 1}$ to pin 10 or pin 15	V_{DD}-0.5	–	V_{DD}	V
	AGC output saturation voltage LOW at I = 0.2 mA		–	1.8	2.3	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Video output						
V_O	video output signal amplitude (Δf = 13.5 MHz p-p)	pin 9 to pin 10 or pin 15	–	1.1	–	V
$V_{O(DC)}$	DC level of video output	pin 9 to pin 10 or pin 15; note 9	3.1	3.5	3.9	V
Z_O	output impedance	pin 9	–	30	50	Ω
Z_L	AC load impedance	pin 9; note 10	600	–	–	Ω
Voltage regulator						
V_{ref}	reference voltage for $\lvert I_{load}\rvert \leq 1$ mA	pin 11; note 11	–	7	–	V
V_{reg}	line regulation 8.1 V ≤ VIN ≤ 9.9 V	pin 11	–	70	–	mV
I_{load}	allowable load current	pin 11	–1	–	0	mA

Notes

1. The supply current is the consumption of the circuit only.
   The current consumption of this application is given by the addition of the supply current of the circuit plus the current consumption of external components in the application given. In this event (Fig.4) the typical current is 80 mA.
2. The circuit of Fig.4 is designed for an input level of 70 dBμV.
   The maximum allowable input level for PLL design is 74 dBμV.
   However, for levels other than 70 dBμV the optimum loop filter values will be different from those given in Fig.4.
3. In the application circuit of Fig.4 the RF input is asymmetrically driven.
   In order to reduce the influence of oscillator signal coupling to the RF inputs, it is recommended to use a symmetrical drive at both inputs.
4. The linearity is specified as the maximum difference between the slope df/dV at the channel centre frequency (480 MHz) and the slope at 480 MHz ± 10 MHz.
5. Measurements with test signals in accordance with CCIR Rec. 473-3; Fm signal with DBS parameters: pre-and de-emphasis in accordance with CCIR Rec. 405-1, 625 lines PAL TV system. Modulator sensitive 13.5 MHz/V at pre-emphasis cross over frequency 1 V(p-p) video signal at pre-emphasis filter input.
6. For the intermodulation measurement, an FM test signal is applied having the following modulating components: 1.5 MHz reference sinewave with a deviation of 9.45 MHz(p-p), 5.5 and 5.75 MHz sinewaves with deviation 5.6 MHz(p-p) (so 4.5 dB below the reference, see Fig.3). At the demodulator output the 2nd order intermodulation is defined according to Fig.3. The video output is loaded with 500 Ω resistor + DC blocking capacitor.
7. The voltage applied at pin 16 is allowed to be higher than the minimum supply voltage (8.1 V).
8. The voltage at the AGC output (pin 1) decreases when the RF input level at pin 13 increases above the adjusted AGC threshold.
9. The DC level at the video output decreases when the RF input frequency increases.
   The DC level at the video output (pin 9) is measured with the VCO switched off because when the oscillator is operating, the DC level is dependent on the application (oscillator into the input).
10. The load impedance must have at least the minimum value for a frequency range from DC to the bandwidth of the i.f. filter (usually 27 MHz) since wide-band noise components will also appear at the video output.
11. It is possible to use the regulator output voltage (pin 11). The maximum current allowed is 1 mA.
    Possible application as voltage reference source for AFC circuit.

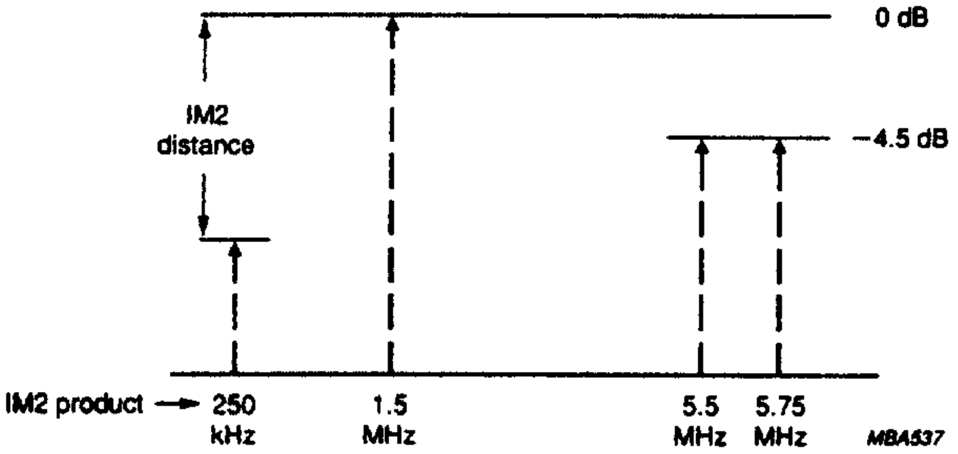


Fig.3 IM2 product.

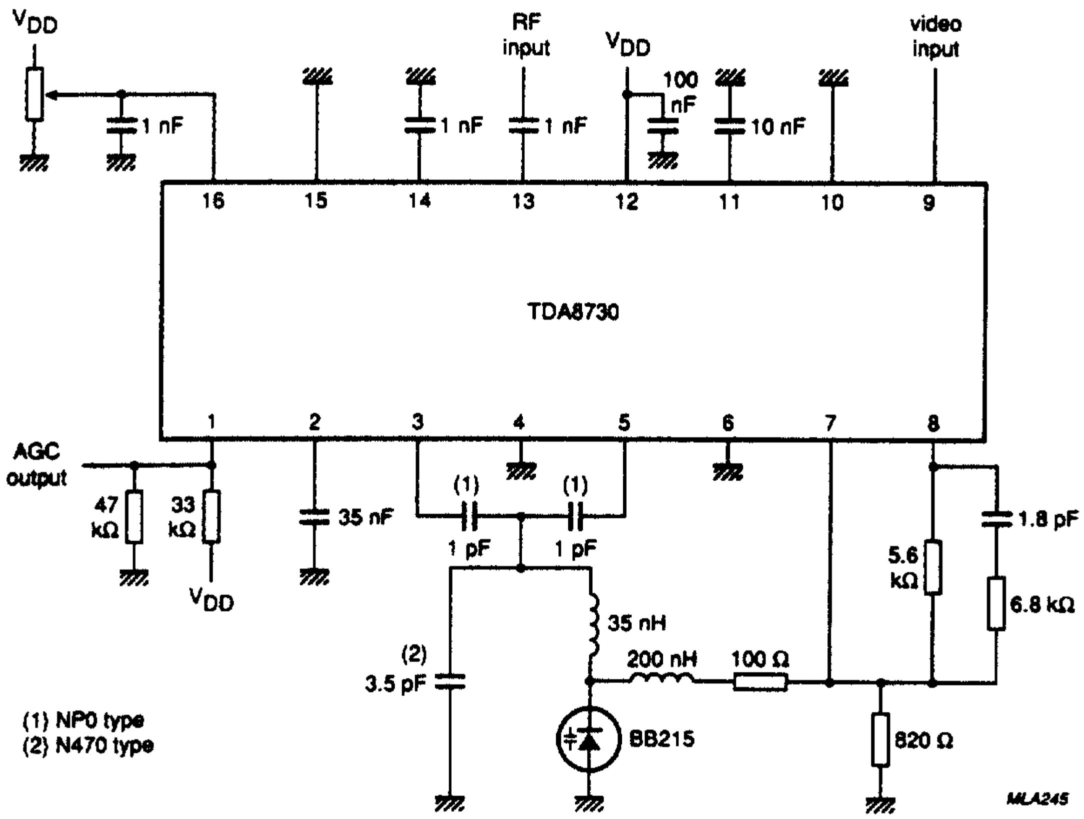
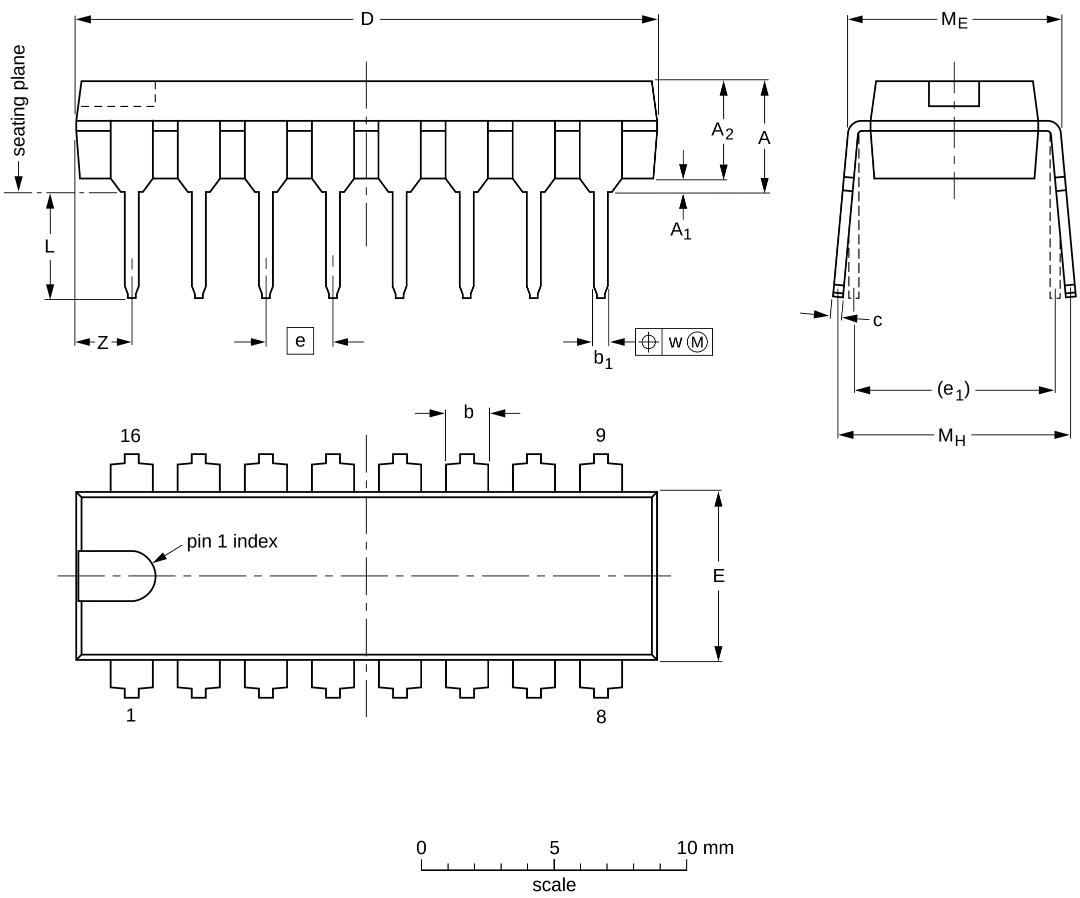


Fig.4 Application information.

PACKAGE OUTLINE

DIP16: plastic dual in-line package; 16 leads (300 mil); long body **SOT38-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	3.7	1.40 1.14	0.53 0.38	0.32 0.23	21.8 21.4	6.48 6.20	2.54	7.62	3.9 3.4	8.25 7.80	9.5 8.3	0.254	2.2
inches	0.19	0.020	0.15	0.055 0.045	0.021 0.015	0.013 0.009	0.86 0.84	0.26 0.24	0.10	0.30	0.15 0.13	0.32 0.31	0.37 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-1	050G09	MO-001AE				~~92-10-02~~ 95-01-19

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

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